IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	:	
Andricacos et al.	:	
Serial No.: 09/760,884	:	Art Unit: 1753
Filed: January 17, 2001	:	Examiner: Brian L. Mutschler
For: Tungsten Encapsulated Copper Interconnections using Electroplating	:	Atty Docket: YOR920000578US1

REPLY BRIEF

Commissioner for Patents
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Sir:

This is an appeal from the Primary Examiner's final rejection of claims 10-22 and 29-30 and in reply to the Examiner's Answer mailed June 25, 2004.

I. Real Party in Interest

The real party in interest is International Business Machines Corporation.

II. Related Appeals and Interferences

There are no other appeals or interferences known to Appellant, Appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's Decision in this Appeal.

III. Status of Claims

Claims 10-22 and 29-30 are pending in the application.

Claims 10-22 and 29-30 were rejected and are the subject of this appeal.

IV. Status of Amendments

The amendment made subsequent to the final rejection has been entered.

V. Summary of Invention

The present invention relates to interconnection wiring on electronic devices such as on integrated circuit (IC) chips and more particularly to encapsulated copper interconnection in integrated circuits.

(page 1, lines 2-5).

In many prior art techniques, copper is electrodeposited on a copper seed layer which in turn is deposited onto a diffusion barrier layer. Both diffusion barrier and Cu seed layer are typically deposited using physical vapor deposition (PVD), ionized physical vapor deposition (IPVD), or chemical vapor deposition (CVD) techniques (Hu et al., Mat.Chem. Phys., 52 1998)5). All of these methods, PVD, IPVD, and CVD require special tooling along with a vacuum.

(page 2, lines 5-10).

In particular, the present invention relates to an electronic structure comprising a substrate having a dielectric layer having a via opening therein; the via opening having a sidewalls and bottom surfaces; a barrier layer deposited on the sidewalls and bottom surfaces of the via opening; copper electrodeposited from a bath having a pH of 12.89 or greater on the barrier layer on the sidewall and bottom surfaces of the via opening.

Another aspect of the present invention relates to a method for fabricating an electronic structure which comprises forming an insulating material on a substrate; lithographically defining and forming recesses for lines and/or via in the insulating material in which interconnection conductor material will be deposited; depositing a barrier layer,

(page 2, lines 18-26).

and electrodepositing copper from a bath having a pH of at least about 12.89 on the barrier layer.

(Page 3, lines 1-2).

Typical barrier layers are tungsten, titanium, tantalum, nitrides thereof and alloys thereof. Also, the barrier layer can include two or more layers (e.g. - W/WN bilayer). The preferred barrier layer comprises tungsten.

(Page 4, lines 5-7).

A copper or copper alloy layer 5 can be deposited directly onto the diffusion barrier layer 4. The copper can be deposited directly on the barrier layer 4 without any additional seed layer by electrodeposition from a plating both having a pH of about 12.89 or more. The copper plating is employed to fill the lines and/or vias openings 3.

(Page 4, lines 14-17).

The technique of the present invention can be used for single and dual damascene structures.

(Page 5, lines 12-13).

The invention further relates to a structure having copper plated directly on a barrier layer without an intervening seed layer and methods for so making. (Original Claim 28).

VI. Issues

Claims 10-14, 16-20 and 29-30 were rejected under 35 U.S.C. § 103(a) over Chen (WO 99/47731 in view of Landau (6,261,433).

Claims 15 and 21-23 were rejected under 35 U.S.C. § 103(a) over Chen (WO 99/47731) in view of Landau (6,261,433) and further in view of Ting (5,969,422).

The issue on appeal is whether the Examiner has established that the cited art fairly teaches each recitation of the present invention.

VII. Grouping of Claims

Claims 10-23 and 29-30 stand or fall together as a group.

VIII. Appellant's Arguments

The present invention discloses and recites limitations that are neither disclosed, recited, nor anticipated by the references cited under 35 U.S.C. § 103(a).

The present invention relates to an electronic device wherein copper is plated directly onto a barrier layer in the absence of an intervening metal seed layer. The cited art relates to plating copper onto a barrier layer having a metal seed layer deposited thereon.

Ting recites:

> A high conductivity interconnect structure is formed by electroplating or electroless plating of Cu or a Cu-base alloy on a seed layer comprising an alloy of a catalytically active metal, such as Cu, and a refractory metal, such as Ta. The seed layer also functions as a barrier/adhesion layer for the subsequently plated Cu or Cu-base alloy. Another embodiment comprises initially depositing a refractory metal barrier layer before depositing the seed layer.[1] (Emphasis mine).

Ting teaches the essential nature of the seed layer:

> A seed layer is required to catalyze electroless deposition or to carry electrical current for electroplating. For electroplating, the seed layer must be continuous. However, for electroless plating, very thin catalytic layers, e.g., less than 100 Å, can be employed in the form of islets of catalytic metal.[2] Ting further teaches a method for depositing the seed layer and also teaches suitable components for a seed layer: In accordance with the present invention, a seed layer comprising an alloy of a refractory metal and one or more catalytically active metals such as nickel (Ni), cobalt (Co), silver (Ag), gold (Au), palladium (Pd), platinum (Pt), rhodium (Rh) or Cu, preferably Cu, is deposited in the opening and on the dielectric interlayer. The seed layer alloy advantageously serves not only as a catalyst or base metal for subsequent electroless plating or electroplating, but as a diffusion barrier preventing Cu from diffusing through the underlying dielectric material, and as an adhesion layer preventing delamination of subsequently electrolessly deposited or electroplated Cu. It has been found that an alloy of a refractory metal and catalytically active metal, such as Cu, exhibits superior step coverage, even in filling openings with high aspect ratios, vis-a-vis Cu alone. Accordingly, by depositing an alloy of a refractory metal and a catalytically active material

[1] U.S. Patent 5,969,422 Abstract.
[2] U.S. Patent 5,969,422 column 4, lines 19-22.

> for subsequent electroless deposition or electroplating of Cu, particularly an alloy of refractory metal and Cu, high aspect ratio openings can be reliably filled with a catalytic seed layer.[3] (Present emphasis).

The Examiner cites Ting as teaching plating copper over a barrier layer (in the presumptive absence of a seed layer: Regarding claim 15 TING et al. disclose a method for forming copper interconnect structures in electronic devices by plating copper over a barrier layer **30**, which is formed on an insulating layer (fig. 3; col. 9, lines 52-65).[4] However, inspection of the section cited by the Examiner reveals Ting does, in fact, teach a seed layer:

> Another embodiment of the present invention is illustrated in FIG. 3, wherein an initial barrier layer 30 is deposited in opening 13 and on dielectric interlayer 10 or optional etch stop layer 12, for additional prevention of Cu migration. Barrier layer 30 can comprise a refractory metal, refractory metal alloy or refractory metal compound, preferably Ta, W or a nitride thereof. Subsequently, catalytic seed layer 14, comprising an alloy of Cu and a refractory metal, is deposited on barrier layer 30 within opening 13 and on dielectric interlayer 11. Cu or a Cu-base alloy 15 is then electrolessly plated or electroplated on Cu-refractory metal catalytic seed layer 14 filling opening 13 and forming a thin layer on dielectric interlayer 11. Subsequent processing then continues in a manner similar to that illustrated in FIG. 2.[5] (Present emphasis).

The passage cited by the Examiner explicitly teaches a catalytic seed layer.

Landau also teaches a seed layer:

> More particularly, the invention provides uniform and void-free deposition of metal onto metal seeded semiconductor substrates having sub-micron, high aspect ratio features.[6]
>
> The method generally comprises physical vapor depositing a barrier layer over the feature surfaces, physical vapor depositing a conductive metal seed layer, preferably copper, over the barrier layer, and then electroplating a conductive metal over the seed layer to fill the structure/feature. Finally, the deposited layers and the dielectric layers are planarized, such as by chemical mechanical polishing (CMP), to define a conductive interconnect feature.[7]

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[3] U.S. Patent 5,969,422 column 6, lines 36-54.
[4] Office Action mailed 10/09/2003 (hereinafter Paper 6).
[5] U.S. Patent 5,969,422 column 9, lines 52-65.
[6] U.S. Patent 6,261,433 Abstract.
[7] U.S. Patent 6,261,433 column 2, lines 24-32.

The Examiner has not cited Landau as teaching the absence of a seed layer.

The Examiner cites Chen as teaching plating copper over either a seed layer or a bare barrier layer.[8] The Chen abstract apparently supports the Examiner by reciting: "electroplate copper directly onto a barrier layer material." However, Chen teaches away from plating copper directly onto a barrier layer. Chen relates to "an alkaline electrolytic copper bath ...used to enhance an ultra-thin copper seed layer which has been deposited on a barrier layer using a deposition process such as PVD."[9] The method of Chen comprises the deposition of "an ultra-thin copper seed layer...on the barrier layer."[10] Chen claims as their invention enhancement of an ultra-thin seed layer as opposed to the "relatively thick seed layer used in the prior art."[11] After presenting difficulties of prior art attempts to use ultra-thin seed layers Chen et al. set forth their invention: The present inventors have found that an ultra-thin seed layer can be employed if it is combined with a subsequent electrochemical seed layer enhancement technique.[12] Chen et al. use Example 1 at page 24-25 to demonstrate the unsuitability of plating copper without prior enhancement of the seed layer. This demonstration teaches away from methods that omit a seed layer.[13]

REPLY TO EXAMINER'S ANSWER

The present invention, as amended, comprises a single independent claim (Claim 10) and claims dependent therefrom. Claim 10 stands rejected under § 103 under Chen (WO '731) in view of Landau and in view of Ting. The present invention plates copper directly onto a barrier layer. The Examiner asserts that WO '731 meets this aspect of the invention by plating copper on a barrier layer in the interstitial spaces between regions of a copper seed layer (the Examiner refers to figs 2B and 2C)[14]. However, WO '731 clearly teaches away from this interpretation; reciting at page 14:

> The use of an ultra-thin seed layer 15 generally introduces its own set of problems. One of the most significant of these problems is the fact that

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[8] Paper 6, page 4, line 7.
[9] WO 99/47731, page 12, lines 11-13.
[10] WO 99/47731, page 13, lines 6-7.
[11] WO 99/47731, page 13, lines 19-20.
[12] WO 99/47731, page 14, lines 13-15.
[13] Teaching away from the invention is a *per se* demonstration of nonobviousness. U.S. v. Adams, 338 U.S.39, 148 U.S.P.Q. 479 (1966).
[14] Examiner's Answer at page 10, lines 9-12.

> such ultrathin layers do not generally coat the barrier layer 14 in a uniform manner. *Rather, voids or non-continuous seed layer regions on the sidewalls, such as at 20, are often present in an ultra-thin seed layer 15 thereby resulting in the inability to properly apply a subsequent electrochemically deposited copper layer in the regions 20.* Further, ultra-thin seed layers tend to include spikes, such as at 21, that impact the uniformity of the subsequent electrolytically deposited metal layer. Such spikes 21 result in high potential regions at which the copper deposits at a higher rate than at other, more level regions. *As such, the seed layer 15 is not fully suitable for the traditional electroplating techniques typically used after application of a seed layer.*
>
> The present inventors have found that an ultra-thin seed layer can be employed if it is combined with a subsequent electrochemical seed layer enhancement technique. To this end, the semiconductor workpiece is subject to a subsequent process step in which a further amount of copper 18 is applied to the ultra-thin seed layer to thereby enhance the seed layer. A seed layer enhanced by the additional deposition of copper is illustrated in fig. 2C. As shown in fig. 2C, void or non-contiguous regions 20 of fig. 2B have been filled thereby leaving substantially all of the barrier layer 10 covered with copper.[15]

The Examiner argues that the regions of barrier exposed by voids in the copper seed layer may be plated. The Examiner supports his interpretation by reference to figures 2B and 2C of WO 731. However, WO '731 clearly teaches away from the Examiner's interpretation: "As such, the seed layer 15 is not fully suitable for the traditional electroplating techniques typically used after application of a seed layer."[16] Moreover, the cited reference uses the very figures cited by the Examiner to enforce the contrary teaching.

RELEVANT CASE LAW ARGUMENTS

As the above argument has demonstrated, with respect to three separate limitation claimed in the present invention, the primary reference, Chen et al., (WO 99/47731), teaches away from the present invention. Ting also teaches away from the present invention by stating that a seed layer is required for plating copper onto a barrier layer.[17] Teaching away from the invention is a *per se* demonstration of nonobviousness. *U.S. v. Adams*, 338 U.S.39, 148 U.S.P.Q. 479 (1966). *A fortiori*, the reference can neither anticipate nor make obvious the present invention.

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[15] WO '751, page 14.
[16] WO '751, page 14, lines 11-12.
[17] U.S. Patent 5,969,422 column 6, line 36.

The mere fact that prior art may be modified in the manner suggested by the Examiner does not make this modification obvious, unless the prior art suggests the desirability of the modification. No such suggestion appears in the prior art in this matter. The Examiner's attention is kindly directed to *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984), *In re Laskowski*, 10 USPQ2d 1397 (Fed. Cir. 1989) and *In re Fritch*, 23 USPQ2d 1780 (Fed. Cir. 1992).

Concerning the above rejection of the claims, the Examiner should be mindful of the following cautionary statement made by the Court in *Grain Processing Corp. v. American Maize-Products Corp.*, 5 USPQ2d 1788 (Fed. Cir. 1988):

> Care must be taken to avoid hindsight reconstruction by using the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the same result of the claims in suit.

Likewise, as stated by the court in *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985):

> It is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claim as a blueprint. When prior art references require selected combination to render obvious a subsequent invention, there must be some reason for the combination, other than the hindsight obtained from the invention itself. It is critical to understand the particular results achieved by the new combination.

In the present situation, no such reasoning for the combination exists in the prior art, and nothing in the prior art would suggest the properties achieved by the present invention. Also, see *In re Fine*, 5 USPQ2d 1596 (Fed. Cir. 1988) wherein the Court stated that "one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." Moreover, it is important to keep in mind that statements in the prior art should not be read out of context when evaluating obviousness. See *In re Wright*, 9 USPQ2d 1649 (Fed. Cir. 1989).

The prior art lacks the necessary direction or incentive to those of ordinary skill in the art to render a rejection under 35 USC 103 sustainable. The prior art fails to provide the degree of predictability of success of achieving the properties attained by the present invention needed to have a rejection under 35 U.S.C. 103 sustained. See *In re Mercier*, 187 USPQ 774 (CCPA 1975) and *In re Naylor*, 152 USPQ 106 (CCPA 1966).

Moreover, the properties of the subject matter and improvements which are inherent in the claimed subject matter and disclosed in the specification are to be considered when evaluating the question of obviousness under 35 USC § 103. See *Gillette Co. v. S.C. Johnson & Son, Inc.*, 16 USPQ2d 1923 (Fed. Cir. 1990), *In re Antonie*, 195 USPQ 6 (CCPA 1977), *In re Estes*, 164 USPQ 519 (CCPA 1970), and *In re Papesch*, 137 USPQ 43 (CCPA 1963).

No property can be ignored in determining patentability and comparing the claimed invention to the prior art. Along these lines, see *In re Papesch*, supra, *In re Burt et al.*, 148 USPQ 548 (CCPA 1966), *In re Ward*, 141 USPQ 227 (CCPA 1964), and *In re Cescon*, 177 USPQ 264 (CCPA 1973).

Conclusion

The above discussion renders it abundantly clear that the Primary Examiner erred in finally rejecting claims 10-22 and 29-30. Therefore, the undersigned respectfully requests the Board to reverse the Examiner and grant claims 10-22 and 29-30.

Respectfully submitted,

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APPENDIX
CLAIMS ON APPEAL

1-9. (Canceled)

10. (Previously presented) A method of fabricating an electronic structure which comprises

forming an insulating material on a substrate;

lithographically defining and forming recesses for lines and/or via having sidewalls and bottom surface in the insulating material in which interconnection conductor material will be deposited;

depositing a barrier layer on sidewalls and bottom surfaces of the recesses;

providing an electroplating bath comprising:

a source of cupric ions,

a complexing agent,

cyanide ions,

a stabilizing agent,

and a pH of at least 12.89;

providing an electrical current sufficient to provide a current density of from about 5 to about 25 milliamps/cm^2; and

electroplating copper directly on said barrier layer.

11. (Original) The method of claim 10 wherein the copper is deposited to provide a thickness of about 10 nanometers to about 100 nanometers.

12. (Original) The method of claim 10 wherein the copper is deposited to provide a thickness of about 20 to about 50 nanometers.

13. (Original) The method of claim 10 wherein the barrier layer is selected from the group consisting of tungsten, alloys of tungsten, titanium, alloys of titanium, titanium nitride, tantalum, tantalum nitride and tantalum silicon nitride.

14. (Original) The method of claim 10 wherein the barrier layer has a thickness of at least about 4 nanometers.

15. (Original) The method of claim 10 wherein the barrier layer is tungsten.

16. (Original) The method of claim 10 wherein the dielectric is silicon dioxide.

17. (Previously presented) The method of claim 10 wherein the recesses have an aspect ratio of greater than 3:1.

18. (Original) The method of claim 10 wherein the electroplating bath is at a room temperature of about 22° C.

19. (Previously presented) The method of claim 10 wherein the source of cupric ions is $CuSO_4$, and the complexing agent is EDTA or a salt thereof.

20. (Original) The method of claim 19 wherein the electroplating bath comprises sodium hydroxide or potassium hydroxide.

21. (Previously presented) The method of claim 10 wherein the electroplating bath further comprises a surfactant.

22. (Previously presented) The method of claim 10 wherein the stabilizer is 2,2' -bipyridyl.

23-28. (Canceled)

29. (Previously presented) The method of claim 10 wherein said current density is 10 to about 20 mA/cm^2.

30. (Currently amended) The method of claim 29 wherein said current density is about 15 $milliamp/cm^2$

31. (Canceled).